



C/M  
2/16/03

2829

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Rincon et al  
Appl. No.: 09/992,065  
Filed: November 21, 2001  
Title: Dual Plane Probe Card ...

Art Unit: 2829  
Examiner: Nguyen  
Docket: TI-32568

7/a  
P. Scott  
2-19-03

Assistant Commissioner  
for Patents  
Box NonFee Amendment  
Washington, DC 20231

MAILING CERTIFICATE	
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 today.	
<i>Gracia Sansom</i>	<i>2-6-03</i>
Gracia Sansom	Date

AMENDMENT

Dear Sir:

In response to the Office Action mailed 11/06/2002, please amend as shown on the attached sheets: "Version with markings to show changes made" and "Clean copy".

REMARKS

Claims 1-16 are pending in the application with claims 1-12 rejected and claims 13-16 withdrawn from consideration. Reexamination and reconsideration are hereby requested.

Claims 1-12 were rejected as anticipated by Kasukabe. The Examiner cited Kasukabe Fig.2.

Applicants reply that amended claim 1 clarifies that the sloped intermediate area is linear (not curved). Kasukabe has a flexible multilayer film 44 which is pressed into position and necessarily is curved between the support by circuit board 50 and the pressing member 43; this has no suggestion of a linear sloped intermediate area.

Respectfully submitted,

*Carlton H. Hoel*  
Carlton H. Hoel  
Reg. No. 29,934  
Texas Instruments Incorporated  
PO Box 655474, M/S 3999  
Dallas, Texas 75265  
972.917.4365

RECEIVED  
FEB 13 2003  
TECHNOLOGY CENTER 2800

1.(amended) A dual plane probe card apparatus for contacting and testing integrated circuit chips including:

- a probe card substrate having first and second major surfaces;
- said probe card substrate offset to form a centrally located horizontal plane, a linear sloped intermediate area, and a peripheral plane parallel to the first horizontal plane;
- a plurality of probe contacts arrayed on the first surface of said central plane in a pattern to mirror the contact pads of a DUT;
- an array of conductive traces adhered to said first substrate surface by a flexible insulating film wherein the traces fan from the probe contacts to conductive vias on the peripheral plane; and
- an array of conductive vias connecting said conductive traces adhered to the first surface to probe head contacts on the second surface.

*a* 1.(amended) A dual plane probe card apparatus for contacting and testing integrated circuit chips including:

- a probe card substrate having first and second major surfaces;
  - said probe card substrate offset to form a centrally located horizontal plane, a linear sloped intermediate area, and a peripheral plane parallel to the first horizontal plane;
  - a plurality of probe contacts arrayed on the first surface of said central plane in a pattern to mirror the contact pads of a DUT;
  - an array of conductive traces adhered to said first substrate surface by a flexible insulating film wherein the traces fan from the probe contacts to conductive vias on the peripheral plane; and
  - an array of conductive vias connecting said conductive traces adhered to the first surface to probe head contacts on the second surface.
-